

# Formation of Controlled Sublithographic Structures

## DESCRIPTION

### BACKGROUND OF THE INVENTION

[Para 1] The field of the invention is that of integrated circuit fabrication, in particular forming sublithographic structures.

[Para 2] In the field of integrated circuit processing, there is relentless pressure to shrink the dimensions of individual features such as lines or holes.

[Para 3] At any given time, the state of lithography has a minimum achievable dimension that is sufficiently reliable to be used commercially.

[Para 4] Workers in the art have constructed "sublithographic" features by fabricating a dummy pillar or block with vertical sides, depositing a sidewall of material on the vertical sides with a thickness less than the minimum ground rule that is available, then removing the pillar selective to the sidewall, thereby leaving the sidewall as a thin vertical member (often called a fin) having a width less than is possible to achieve using the standard lithographic groundrules.

[Para 5] The sidewall is selected for its ability to form a thin fin that is strong enough to survive the processing, not for its electrical properties. Accordingly, the fin is often used as a hardmask to pattern a lower layer that is not as durable, but has better electrical properties.

[Para 6] A conventional process of forming thin vertical fins in the prior art includes the following;

- (1)Form a stack of the structure material that will form the fins (silicon), hardmask (oxide) and temporary or dummy layer (silicon);
- (2)Etch temporary pillars in the dummy layer that will support the sidewalls;
- (3)Deposit a conformal (nitride) spacer film over the dummy pillars having a thickness that will define the width of the final structures;
- (4)Directionally etch the horizontal portions of the conformal spacer film, exposing the top of the dummy material and the hardmask;
- (5)Planarize the common top surface of the dummy material and the sidewalls;
- (6)Remove the dummy pillars, leaving the sidewalls;
- (7)HF clean the oxide hardmask after silicon removal;
- (8)Etch the hardmask, using the sidewalls as a mask;
- (9)Directionally etch the structure layer, using the hardmask to define the final structure, thereby forming the fins.

[Para 7] The sequence according to the prior art is illustrated in relevant format in Figures 1 – 4, in which;

[Para 8] Figure 1 shows a typical starting material comprising a wafer substrate 10 that, in this case, is an SOI wafer having buried oxide insulator (BOX) 15 above which there is a device layer 20, also referred to as the structure layer, that will contain the final sublithographic structure.

[Para 9] An oxide hardmask 30 has been thermally grown or deposited on the top of the structure layer. The sidewall image transfer process forms a sidewall of sublithographic thickness on a dummy pillar formed in a dummy layer 50 and transfers the image to the hardmask, thereby defining a sublithographic hard mask that can be used to define the structure in the structure layer.

[Para 10] Such a process is often used to define the fins for a FINFET, but can also be used for other structures such as capacitor plates,.

[Para 11] Figure 2 shows the result of defining the dummy pillars 55, in which the pillars have a width denoted by bracket 52 that defines the pitch between the sidewalls and therefore the structure pitch between the pairs of final structures that will be formed. When the dummy pillars are defined by a lithographic process, the smallest value of distance 52 will be set by the limit of current lithographic technology.

[Para 12] Bracket 54 denotes the pitch of adjacent pillars and will also have a lower limit set by the current ground rules. The distance between a final structure resulting from a right sidewall on the pillar on the left in Figure 2 and a corresponding structure resulting from the left sidewall on the pillar on the right in Figure 2 will be distance 54 minus distance 52.

[Para 13] When the dummy material is amorphous silicon, the pillars 55 may be defined by a reactive ion etch using CF<sub>4</sub>, CHF<sub>3</sub>, CH<sub>2</sub>F<sub>2</sub>, CH<sub>3</sub>F, O<sub>2</sub>, Ar chemistry.

[Para 14] Figure 3 shows the result of depositing a conformal layer of nitride 60 in a conventional CVD process. The thickness of layer 60 on the sides of pillars 55 (the sidewall thickness) will define the width of the oxide hardmask and thus also define the width of the final structures.

[Para 15] Figure 4 shows the result of a directional nitride spacer etch using CF<sub>4</sub>, CHF<sub>3</sub>, CH<sub>2</sub>F<sub>2</sub>, CH<sub>3</sub>F, O<sub>2</sub>, Ar chemistry that removes the horizontal components of film 60 as shown. Figure 4 shows the result of an overetch at the top of the pillars 55 that is required to assure that the lower horizontal component of film 60 resting on the hardmask 30 has been removed. Prior art methods typically planarize the top surface of the pillars and the top surface of the sidewalls.

[Para 16] Circles 32 in Figure 4 indicate areas where the hardmask film 30 has been damaged by the nitride spacer etch. These areas will etch faster in the etch that defines the hardmask than the areas underneath pillars 55 that are protected by the pillars during this etch. The result of this asymmetry is that the hardmask will not have a flat top (or vertical sides) but will have a slanting top where the damaged oxide was removed more quickly. That defect in the hardmask results in poor quality of definition in the final structures.

[Para 17] Typically, the spacer transfer etch that defines the hard mask using the nitride spacers as a mask is a directional RIE etch. Even though directional, that etch attacks the oxide laterally in the area 32, resulting in the tapered hard mask.

[Para 18] This approach has a number of problems, as would be expected of an attempt to produce a smaller dimension than can be reliably produced using standard techniques.

[Para 19] In particular, transferring the sidewall image to the hard mask layer has been subject to a problem that the etching step that defines the sidewall damages the hardmask layer slightly, compared with the portion of the hard mask layer that is protected by the pillar. When the sidewall image is transferred to the hardmask, there can be differential etching because of the previous differential damage. That differential etching, in turn, can produce a hardmask that is not symmetric and that, in turn, produces a fin that is not up to standard.

[Para 20] An additional problem is that standard technology requires at least one planarization step that is both expensive and prone to cause defects in the material.

## SUMMARY OF THE INVENTION

[Para 21] The invention relates to a sidewall image transfer process for forming sublithographic structures in integrated circuit fabrication that adds a hardmask protective layer that eliminates asymmetric damage to the hardmask during a dry etch step.

[Para 22] A feature of the invention is the formation of sidewalls on a dummy pillar to define the sublithographic width of the final structure.

[Para 23] Another feature of the invention is the removal of horizontal components of the sidewall film in a two-step nitride spacer etch process that avoids use of the conventional HF clean after silicon removal.

[Para 24] Yet another feature of the invention is the symmetric and controlled formation of the hard mask used to pattern the final structure.

[Para 25] Yet another feature of the invention is a double sidewall image transfer process, in which the dummy pillar is a sidewall, thereby permitting the pitch between the final structures to be sublithographic.

## BRIEF DESCRIPTION OF THE DRAWINGS

[Para 26] Figures 1 – 4 shows aspects of the prior art.

[Para 27] Figures 5 – 14 show steps in a version of the invention.

[Para 28] Figures 15 – 20 show steps in an alternative version of the invention.

## DETAILED DESCRIPTION

[Para 29] Referring now to Figure 5, there is shown a stack for use with the invention in which:

[Para 30] substrate 10 is a silicon wafer having an SOI layer 15 and a device layer 20. Other wafers, such as bulk silicon, SiGe alloy, GaAs or others may also be used. In this example, the structure layer 20, which will form the final structure, is nominally 20 – 30 nm thick.

[Para 31] Oxide hardmask 30 performs the same function as hardmask 30 in the prior art – defining the pattern in structure layer 20. The hard mask layer is etched according to the invention to improve the symmetry of the final structure. Layer 30 is illustratively 20 – 30 nm thick. The desired thickness will vary with the thickness of the structure to be etched.

[Para 32] Protective nitride layer 40, illustratively 20nm, is sufficiently thick to prevent damage to the hard mask during the etch and the required overetch of layer 50.

[Para 33] Amorphous silicon layer 50 is illustratively 100 – 150 nm thick. The thickness of this layer will depend on the desired height of the final structure.

The sidewalls have to last during the patterning of the hardmask and the hardmask has to last during the patterning of the final structure.

[Para 34] Figure 6 shows the result of patterning the dummy pillars 55 that will support the nitride sidewalls. Dimensions 52 and 54 define the same spacing between sidewalls and between groups of sidewalls as in Figure 2.

[Para 35] Figure 7 shows the result of depositing a conformal nitride 60 to form the sidewalls.

[Para 36] Figure 8 shows the result of a directional RIE that removes the nitride 60 from the horizontal surfaces on the top of pillars 55 and on the protective layer 40.

[Para 37] Figure 9 shows the result of a wet etch that removes the amorphous silicon pillars 55 selective to nitride 60, leaving nitride sidewalls 65 having a width 67 that will be the width of the oxide hardmask.

[Para 38] A beneficial aspect of the invention is that the stack is now symmetric on both sides of each sidewall 65. Protective layer 40 has been present over hardmask layer 30 and symmetric with respect to the sidewalls 65. It does not matter if there is a residual amount of layer 60 because it will be removed along with layer 40.

[Para 39] Figure 10 shows the result of removing layer 40 in a directional RIE that will also remove some of the top of sidewalls 65. This is the second step



of a two-step removal of the nitride above the oxide hardmask, the first step being shown in Figure 8. The remaining elements 45 of layer 40 will be used to pattern the hardmask layer 30, as shown in Figure 11.

[Para 40] Advantageously, the area on the left and right of sidewalls 65 are both the nitride layer 40. If there is any damage to the hardmask layer 30 at the end of the nitride removal process when there is little or no nitride left, it will be symmetric.

[Para 41] There will be some slight damage to oxide layer 30 during an overetch, when the oxide is exposed to the etch, but it will be symmetric.

[Para 42] No HF clean of oxide 30 is necessary before patterning the oxide because the oxide was not exposed to the etch during silicon removal.

[Para 43] Figure 10 shows bracket 52 and bracket 54 denoting the same distances as in the prior art.

[Para 44] Figure 11 shows the result of patterning and transferring the sidewall image to the oxide hardmask, leaving isolated mask elements 35. Illustratively the patterning is done with a directional RIE using a C<sub>4</sub>F<sub>8</sub>, Ar, CHF<sub>3</sub> chemistry, stopping on the silicon structure layer 20.

[Para 45] Figure 12 shows the result of an optional step in which nitride sidewalls 65 are stripped, illustratively in phosphoric acid. Such a strip takes

fab resources and need only be done when leaving the sidewalls would interfere with later steps. For example, the nitride pillars have a high aspect ratio and the combination of the nitride pillars and the oxide will have an even higher aspect ratio. The higher the aspect ratio, the greater the danger of mechanical breakage, which can cause defects and even a domino effect. If the oxide mask provides sufficient protection for the patterning, then stripping the nitride pillars removes a source of defects.

[Para 46] Figure 13 illustrates the result of another optional step in which a non-critical block mask is used to remove one of the mask elements 35, denoted by the dotted circle 37. This step may be used when the circuit calls for an odd number of structures.

[Para 47] Figure 14 illustrates the result of etching the structure layer 20 to define a set of fins 25, stopping on BOX 15.

[Para 48] Fins 25 may be used to form the source, drain and body in FINFETs, with or without optionally defining blocks in front of and behind the plane of the paper that tie the fins 25 together, giving mechanical strength and connecting the fins electrically in parallel.

[Para 49] The fins 25 may also be used as capacitor plates, diodes, vertical connecting elements (with appropriate doping), and micro-mechanical structures of various sorts.

[Para 50] In the case of FINFETs, further processing steps such as those illustrated in copending patent application S/N 10/731,584, Docket No.

YOR920030380US1, assigned to the assignee hereof and incorporated by reference, may be used to form the transistors.

[Para 51] An alternative version of the invention is illustrated starting with Figure 15, in which the pillars on which the final sidewalls are based are themselves sidewalls – i.e. a double sidewall process.

[Para 52] Figure 15 shows the result of forming amorphous silicon first level pillars 55, as in Figure 6. Substrate 10, BOX 15, structure layer 20, oxide hardmask layer 30 and protective nitride layer 40 are the same as in the previous version of the invention.

[Para 53] In this example, the structure layer 20, which will form the final structure, is nominally 20 – 30 nm thick.

[Para 54] Oxide hardmask 30 performs the same function as hardmask 30 in the prior art – defining the pattern in structure layer 20. The hard mask layer is etched according to the invention to improve the symmetry of the final structure. Layer 30 is illustratively 20 – 30 nm thick. The desired thickness will vary with the thickness of the structure to be etched.

[Para 55] A conformal layer of oxide 160 is deposited to a thickness that will define the pitch between the final sidewalls.

[Para 56] Figure 16 shows the result of an oxide spacer etch, in which the horizontal portions of layer 160 have been removed in a directional RIE, using C4F8, Ar, CHF3 chemistry, leaving oxide pillars 165. The silicon pillars 55 have a thickness 56, so the smallest pitch of the oxide pillars is distance 56 plus the thickness of the layer 160. The pitch between adjacent pairs of oxide pillars is distance 58.

[Para 57] Figure 17 shows the result of stripping the amorphous silicon dummy layer in an isotropic dry etch or a wet etch such as KOH or NH4OH based chemistry, leaving the oxide pillars 165. The thickness of the pillars 165 is distance 167 and distances 56 and 58 are as discussed above.

[Para 58] Figure 18 shows the result of depositing a conformal layer of nitride 170 over oxide second level pillars 165.

[Para 59] Figure 19, similar to Figure 8, shows the result of a directional RIE that removes the horizontal components of the conformal nitride layer 170, leaving the vertical sidewall members 175. The thickness of sidewalls 175 is denoted by distance 177, nominally the same as the thickness of the final structure formed in layer 20. Bracket 152 denotes the smallest pitch of the structures that will be formed in layer 20. Bracket 154 denotes the pitch of pairs of the structures – i.e. of the first level of sidewalls. It is the same as distance 56 in Figure 17.

[Para 60] Figure 20, similar to Figure 9, shows the result of stripping the oxide temporary pillars 165.

**[Para 61]** The remaining steps in this alternative process are similar to those shown in Figures 10 to 14. The sidewalls 175 are used to pattern layer 40.

**[Para 62]** The combined nitride sidewall/layer 40 is used to pattern oxide layer 30, resulting in a sublithographic hardmask that has a spacing set by the sidewalls on temporary pillars 165, so that the spacing also will be sublithographic in this version of the invention.

**[Para 63]** Structure layer 20 is patterned with the oxide hard mask as before, resulting in a structure similar to that of Figure 14, but with smaller spacing.

**[Para 64]** The further steps in this version of the invention – building a structure that uses the fins defined as set forth above – will be the same as for the previous embodiment of the invention.

**[Para 65]** While the invention has been described in terms of a single preferred embodiment, those skilled in the art will recognize that the invention can be practiced in various versions within the spirit and scope of the following claims.